REMARKS

Claims 1-32 are pending. By this Amendment, claims 1 and 27 are amended. Applicants acknowledge with appreciation the Examiner's indication that claims 3, 11-13 and 16-17 are drawn to allowable subject matter. In view of the allowability of the claims from which these claims depend, described below, applicants have maintained these claims in their original dependent form.

Claims 1-2, 4-10, 14-15, 18, and 20-26 were rejected under 35 U.S.C. 102(e) as allegedly being anticipated by published patent application US 2004/0245011 (Amparan et al.). These rejections are respectfully traversed.[1] The present invention differs fundamentally from the Amparan et al. system.

Claims 1-23 of the present application are directed to methods for generating, through electronic data processing (e.g., using a computer-aided-design/engineering system), a split power plane of a multi-layer printed circuit board. The inventive methods utilize an approach that permits crossover of different voltage wireframes to be automatically minimized or eliminated, thus avoiding or reducing the need to manually avoid crossovers through the routing of traces to different PCB layers and/or moving components or vias. In conjunction with reducing or eliminating crossover, the inventive methods also permit a designer to ensure that the traces provided for electrical power distribution will have sufficient width to handle the electrical (e.g., current (*I*)) requirements of the different segments of the wireframe, as determined by the electrical components to be connected on each segment.

[1] While the Office Action does not explicitly reject claims 27-32, discussions regarding these claims provided in the Office Action suggest that perhaps the Examiner intended to include these claims in the rejection. Accordingly, these Remarks address the patentability of claims 27-32 as well.

Known computer-aided-design (CAD) based PCB autorouters will graphically illustrate desired power plane connections with straight line paths corresponding to the shortest distances between the placed components. As described in the application, each connection between any surface mount device (SMD) on the outside of the PC board to the inner layer power plane will be made by means of a via, and a through-hole device will make its connection to this same plane by means of its plated barrel. With existing systems, the PCB designer basically has two options for proceeding in creating split power planes. These are described below.

Option 1 (conductive areas): The user will pre-define polygonal shaped conductive areas with the goal of each shape containing all connections of a common power potential. Depending on the quantity of potentials needed on the split power plane, and the present placement locations of the components, this can require several iterations of editing these polygonal shapes. There is no guarantee that upon completing these shapes that the current (*I*) handling to all connections will be sufficient, especially considering that the conductive areas will be interrupted by vias and through-hole device connections.

Option 2 (conductive traces): Instead of the user creating polygonal shapes, the autorouter may apply a single user-defined trace width (e.g., 0.030") that will be used for all trace connections of the split power plane. Depending on the current (*I*) requirements for the potentials, if the trace width is based on the maximum current required by the circuit, the autorouter may not be able to complete the remaining signal connections that must be made after the power connections are established, due to the limited remaining area and the need to avoid the traces in placement of those connections. If the trace width is based on some other value that does not consider the maximum current needed by a device, the risk significantly increases that

the circuit will not work as designed because the current needs of a device (or devices) is not provided. Therefore the user would need to be involved in a tedious, iterative process of customizing trace widths without introducing crossovers for each power potential.

Building on the approach of option 2 just described, the present invention has the potential to dramatically lessen the burden placed on the PCB designer, because the wireframe can be iteratively enhanced through data processing, and it can be assured that the current requirement needs between the power sources and each power source's respective loads will be met.

Starting, e.g., from the conventional straightline (minimum distance) representation of connections of the existing autorouter (typically having abundant crossover), the method of the present invention generates a plurality of initial voltage wire frames and then an enhanced set of voltage wire frames, to arrive at a split plane wireframe having no or a reduced quantity of crossover. Once this enhanced split plane wireframe is established, the designer can be afforded the opportunity (as necessary) to make any further adjustments in order to achieve a "clean" wireframe entirely free of crossover. The inventive method further enables a determination of trace widths in accordance with stored electrical requirements of associated components available for retrieval by the system. In this manner, the designer is relieved of the otherwise manual task of verifying that the plane area is free of unacceptible limitation caused, e.g., by (a) insufficient area, or (b) an area heavily populated with signal vias that significantly reduces its true current (*I*) handling capability.

In contrast, Amparan et al. disclose a method wherein a potential field of a PCB power plane is calculated by assigning potential values to components and solving for potential field values at a plurality of locations between the components. Amparan et al. disclose a contour

solver that computes a potential field and determines boundaries so that nodes with the same value are within the same boundary. Traces are established and expanded within the bounded areas. See, e.g., Abstract and paras. 0017-18.

The present invention differs fundamentally from the Amparan et al. system, in that Amparan et al. do not take steps to generate a plurality of initial voltage wireframes and then an enhanced set of wireframes having no or a reduced quantity of crossover. Since Amparan et al. define distinct non-shorting potential field regions within which traces will be established (see, e.g., para. 0033; Fig. 10), crossover is inherently avoided from the outset, and the occasion to eliminate or reduce crossover following a step of generating voltage wire frames does not arise.

Nor do Amparan et al. teach or suggest a step of determining a trace width for segments of a split plane wireframe in accordance with stored electrical requirements of associated components. Once Amparan et al. have established their bounded regions corresponding to common voltages, an upper limit on the widths of the traces is inherently established; depending on the routing densities, it might not be possible to achieve a trace width within the bounded region sufficient to handle the current (*I*) requirements of the associated components. In any event, no provision is taught by Amparan et al. for making this determination and/or satisfying it. This is a shortcoming that may be avoided with the present invention.

Moreover, Amparan et al.'s conceptual disclosure fails to deal with practical constraints on the design process, including the strong preference (if not the need) for the use of traces arranged orthogonally or at 45° angles with respect to each other in the final design. The iterative approach of the present invention permits early introduction in initial wireframes of such a practical desirable configuration (see, e.g., application Fig. 5), which may then be enhanced to reduce crossover. This facilitates creation of a practical final design, which will

permit efficient utilization of known equipment (e.g., a Gerber photo-plotter) used in the PCB preproduction tooling preparation. In contrast, traces having complex curvatures corresponding to the bounded (non-shorting) regions 1010, 1020 and 1030 of Amparan et al.'s Fig. 10 could not be efficiently photo-plotted with conventional equipment.

As described above, claim 1 is not anticipated by Amparan et al. Claims 2, 4-10, 14-15, 18 and 20-26 depend from claim 1 and are also not anticipated for at least the above reasons. Accordingly, allowance of claims 1-2, 4-10, 14-15, 18, and 20-26 is respectfully requested.

Paralleling claim 1, claim 27 recites a processor configured to generate a plurality of initial voltage wireframes and a set of enhanced wireframes having no or a reduced quantity of crossover, and to determine a trace width in accordance with stored electrical requirements of associated components. As described above in connection with claim 1, this feature is not taught or suggested by Amparan et al. Claims 28-32 depend from claim 27 and are allowable based on that dependency.

Claim 19 was rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Amparan et al. in view of "Channel Routing in Manhattan-Diagonal Model" (Das). Claim 19 depends from claim 1. However, Das is cited only for the feature of "routing with vertical, horizontal and diagonal with 45 degree connections" (Office Action, paragraph 20), and clearly does not make up for the above-noted fundamental deficiencies of Amparan et al. Thus, claim 19 is patentable over Amparan et al. and Das.

Based upon the foregoing, applicants respectfully submit that the pending claims are patentably distinguished over the applied Amparan et al. published patent application. Applicants arguments distinguishing over Amparan et al. should not, however, be construed to be an acknowledgment or admission that the reference in fact constitutes prior art to the present

invention. To the contrary, applicants wish to note for the record that their invention predates the June 3, 2003 filing date of the Amparan et al. patent application. If called upon to do so, applicants would be in a position to submit testimonial and documentary evidence to "swear behind" Amparan et al. and thereby remove it as prior art. Applicants deem this step to be unnecessary at present, but expressly reserve the right to make such a submission as future circumstances may warrant.

For all of the foregoing reasons, it is respectfully submitted that this application is now in condition for allowance. Should the Examiner believe that anything further is desirable in order to place the application in even better for allowance, he is respectfully urged to telephone applicants' undersigned representative at the below-indicated number.

Respectfully submitted,

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